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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,470	07/15/2003	Lawrence T. Clark	MP1494	8637

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EXAMINER	
SUGENT, JAMES F	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/620,470	CLARK, LAWRENCE T.	
	Examiner	Art Unit	
	James F. Sugent	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *18-20 and 22* is/are allowed.

6)☒ Claim(s) *1-7 and 9-17* is/are rejected.

7)☒ Claim(s) *16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is sent in response to Applicant's Communication received February 2, 2007 for application number 10/620,470 originally filed July 15, 2003. The Office hereby acknowledges receipt of the following and placed of record in file: amended claims 1-22 (wherein claims 8 and 21 are canceled) presented for examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Woods et al. (U.S. Patent No. 7,058,834 B2) (hereinafter referred to as Woods) in view of Stapleton et al. (U.S. Patent No. 6,574,577 B2) (hereinafter referred to as Stapleton).

As to claim 1, Woods discloses a method comprising: providing power to an integrated circuit (IC) (130) during an active mode (column 3, lines 12-23); moving an integrated circuit state of the IC into on-die storage (memory 270 within ISPRM 160) of the IC (column 4, lines 22-29 and column 4, lines 38-47 and column 7, lines 3-32); and, disabling power to on-die combinational circuitry (SPA) during a low power mode (sleep state) by disrupting power supplied from an external power supply regulator to the IC (column 4, lines 48-53 and column 2, line 49 thru column 3, line 2 and column 2, lines 1-10).

Woods fails to disclose the power being disabled externally.

Stapleton teaches a power control method that externally disables power (via 11) to an IC (12) (column 1, lines 40-57). Stapleton further teaches a voltage regulator (14) that stops delivering power (Vccp) to the IC when another input voltage (Vtt) is de-asserted (column 2, lines 38-50). Stapleton further teaches the additional benefit of ensuring a proper voltage is delivered thus preventing an improper, harmful voltage level to a chip (column 1, lines 15-26 and column 2, lines 49-57).

It would have been obvious to one of ordinary skill of the art having the teachings of Woods and Stapleton at the time the invention was made, to modify the method of Woods to include the ability of disabling power externally as taught by Stapleton. One of ordinary skill in the art would be motivated to make this combination of including the ability to externally disable power in view of the teachings of Stapleton, as doing so would give the added benefit of ensuring a proper voltage is delivered thus preventing an improper, harmful voltage level to a chip (as taught by Stapleton above).

As to claim 2, Woods in combination with Stapleton taught the method in claim 1, as shown above. Stapleton further teaches the method wherein disabling power further includes tri-stating an output of a power supply regulator that provides power to the on-die combinational circuitry (column 2, lines 38-50).

As to claim 3, Woods in combination with Stapleton taught the method in claim 1, as shown above. Stapleton further teaches the method wherein disabling power further includes gating an off-die clamp to disrupt power supplied from an external power supply regulator to the on-die combinational circuitry (column 4, lines 15-51).

As to claim 4, Woods in combination with Stapleton taught the method in claim 1, as shown above. Woods further teaches the method wherein disrupting the power further includes gating an on-die clamp (column 6, line 59 thru column 7, line 2).

As to claim 5, Woods in combination with Stapleton taught the method in claim 1, as shown above. Woods further teaches the method including reapplying power after the integrated circuit receives an interrupt (column 8, lines 11-30).

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Woods in view of Stapleton as applied to claim 1 above, and further in view of Borkar et al. (U.S. Patent No. 6,484,265 B2) (hereinafter referred to as Borkar).

As to claim 6, Borkar teaches a power regulation method for a processor. The method teaches supplying power from a power supply regulator (118) along a path (132) to circuitry (114) and providing a feedback signal (126) from the path (132) to the power supply regulator (column 2, line 63 thru column 3, line 11 and column 4, lines 57-67 and column 6, lines 1-7). Borkar has the additional feature of maintaining and managing the

temperature and frequency of the circuit to manage and conserve power (column 2, lines 49-60).

It would have been obvious to one of ordinary skill of the art having the teachings of Woods, Stapleton and Borkar at the time the invention was made, to modify method of Woods to include a feedback signal to the regulator to maintain power as taught by Borkar. One of ordinary skill in the art would be motivated to make this combination of including a feedback signal to the regulator to maintain power in view of the teachings of Borkar, as doing so would give the added benefit of maintaining and managing the temperature and frequency of the circuit to manage and conserve power (as taught by Borkar above).

Claims 7 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stapleton (as cited above) in view of Heimbigner (U.S. Patent No. 4,363,978) (hereinafter referred to as Heimbigner).

As to claim 7, Stapleton discloses method comprising: forcing a high impedance state on an output of a power supply regulator (11) that is coupled to a power pin of an integrated circuit (12) (column 1, lines 40-57 and column 2, lines 38-50), wherein forcing the high impedance state includes de-asserting a drive pin (from Vtt) coupled to a gate of a power transistor to force the high impedance state on the output of the power supply regulator (column 2, lines 38-67 and column 3, lines 18-31).

Stapleton fails to teach the power transistor being a MOS power transistor.

Heimbigner teaches a method that uses a tri-state power driver to gate power to a load. The power driver (96) uses to CMOS transistors to deliver the load in three states of

operation (column 1, line 65 thru column 2, line 23). Heimbigner has the additional feature of further reducing power delivered to a circuit (column 1,lines 31-36).

It would have been obvious to one of ordinary skill of the art having the teachings of Stapleton and Heimbigner at the time the invention was made, to modify method of Stapleton to include the power transistor being a MOS power transistor as taught by Heimbigner. One of ordinary skill in the art would be motivated to make this combination of the power transistor a MOS power transistor in view of the teachings of Heimbigner, as doing so would give the added benefit of further reducing power delivered to a circuit (as taught by Heimbigner above).

As to claim 10, Stapleton in combination with Heimbigner taught the method in claim 7, as shown above. Stapleton further teaches the method comprising: timing the de-assertion to avoid high voltages on a supply inductor coupled between the output of the power supply regulator and the power pin of the integrated circuit (Abstract and column 2, lines 1-10).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stapleton in view of Heimbigner as applied to claim 7 above, and further in view of Cruz (U.S. Patent No. 6,754,692 B2) (hereinafter referred to as Cruz).

As to claim 9, Cruz teaches a power distribution circuit (100) that includes a diode (140) which keeps current from flowing into a circuit's power supply system which is inclusive of a MOS transistor (170) (column 2, lines 24-60 and column 6, lines 14-29). Cruz further teaches the additional benefit of electronically isolating power buses from power domains (column 1, lines 33-53 and column 2, lines 49-60).

It would have been obvious to one of ordinary skill of the art having the teachings of Stapleton and Cruz at the time the invention was made, to modify power supply regulator of Stapleton to include a diode to a source MOS power transistor as taught by Cruz. One of ordinary skill in the art would be motivated to make this combination of including a diode in the power supply regulator in view of the teachings of Cruz, as doing so would give the added benefit of electronically isolating power buses from power domains (as taught by Cruz above).

Claims 11 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harris, II et al. (U.S. Patent No. 5,867,719) (hereinafter referred to as Harris) in view of Woods (as cited above).

As to claim 11, Harris discloses circuit comprising: a first terminal (Vdd 132) of an integrated circuit (IC) coupled to receive power for on-die combinational circuitry when the integrated circuit is in an active mode and to not receive power when the integrated circuit is in a low power mode (Abstract and column 1, line 65 thru column 2, line 24); and, a second terminal (Vstby 130) to receive power supplied to circuitry for low power state of the IC when the integrated circuit is in the low power mode (standby), wherein the second terminal provides power to memory(106) (column 2, lines 27-67).

Harris does not disclose receiving power supplied to circuitry for low power state retention of the IC when the integrated circuit is in the low power mode, wherein power is provided to low-leakage memory that stores the logical state.

Woods teaches a circuit state save and restore method for an IC. Woods further teaches the circuit receiving power supplied to circuitry (ISPRM 160) for low power state retention of the IC when the integrated circuit is in the low power mode (sleep state),

wherein power is provided to low-leakage memory (memory 270 within ISPRM 160) that stores the logical state (column 4, lines 22-29 and column 4, lines 38-47 and column 7, lines 3-32). Woods has the additional benefit of having a state save and restore that is quick and efficient without the need of hardware or software rebooting (column 2,lines 35-42).

It would have been obvious to one of ordinary skill of the art having the teachings of Harris and Woods at the time the invention was made, to modify circuit of Harris to include the ability to save the state of the circuit to memory as taught by Woods. One of ordinary skill in the art would be motivated to make this combination of including the ability to save the state of the circuit to memory in view of the teachings of Woods, as doing so would give the added benefit of having a state save and restore that is quick and efficient without the need of hardware or software rebooting (as taught by Woods above).

As to claim 17, Harris in combination with Woods taught the circuit in claim 11, as shown above. Woods further teaches the circuit further comprising: a transistor (170) internal to the integrated circuit to gate the power received at the first terminal and float an internal power conductor connected to combinational logic (column 6, line 50 thru column 7, line 2).

Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harris in view of Woods as applied to claim 11 above, and further in view of Stapleton (as cited above).

As to claims 12 and 13, Stapleton teaches a power control method that externally disables power (via 11) to an IC (12) (column 1, lines 40-57) wherein a transistor (within 11) external to the integrated circuit to gate the power received at the first terminal and

wherein the transistor is coupled to a power regulator (14) and switched off when the integrated circuit is in the low power mode (column 2, lines 38-50). Stapleton further teaches the additional benefit of ensuring a proper voltage is delivered thus preventing an improper, harmful voltage level to a chip (column 1, lines 15-26 and column 2, lines 49-57).

It would have been obvious to one of ordinary skill of the art having the teachings of Harris, Woods and Stapleton at the time the invention was made, to modify the circuit of Harris to include the ability of disabling power externally as taught by Stapleton. One of ordinary skill in the art would be motivated to make this combination of including the ability to externally disable power in view of the teachings of Stapleton, as doing so would give the added benefit of ensuring a proper voltage is delivered thus preventing an improper, harmful voltage level to a chip (as taught by Stapleton above).

Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harris in view of Woods as applied to claim 11 above, and further in view of Borkar (as cited above).

As to claims 14 and 15, Borkar teaches a power regulation method for a processor. The method teaches supplying power from a power supply regulator (118) along a path (132) to circuitry (114) and providing a feedback signal (126) from the path (132) to the power supply regulator (column 2, line 63 thru column 3, line 11 and column 4, lines 57-67 and column 6, lines 1-7). Borkar further teaches a feedback signal (122) taken from within the IC (column 4, lines 21-26). Borkar has the additional feature of maintaining and managing the temperature and frequency of the circuit to manage and conserve power (column 2, lines 49-60).

It would have been obvious to one of ordinary skill of the art having the teachings of Harris, Woods and Borkar at the time the invention was made, to modify method of Harris to include a feedback signal to the regulator to maintain power as taught by Borkar. One of ordinary skill in the art would be motivated to make this combination of including a feedback signal to the regulator to maintain power in view of the teachings of Borkar, as doing so would give the added benefit of maintaining and managing the temperature and frequency of the circuit to manage and conserve power (as taught by Borkar above).

Allowable Subject Matter

Claim 16 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 18-20 and 22 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: in re independent claim 18, Lu discloses: an IC having a power terminal coupled through an external transistor to an output of a power supply (column 2, line 40 thru column 3, line 67 and column 5, lines 47-55); and, a multiplexer to selectively connects signals to the power supply (column 2, line 63 thru column 3, line 4). However, the limitation wherein the multiplexer selectively connects an external power signal supplied at a pin of the integrated circuit, an internal power signal of the integrated circuit, and a power signal supplied to the external control transistor to the power supply is not taught by Lu and could not be found in further Examiner search.

Response to Arguments

Applicant's arguments with respect to claims 1-6 and 11-17 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments, see pages 8 and 9 of Applicant's Arguments/Remarks, filed February 2, 2007, with respect to the rejection(s) of claim(s) 7, 8 and 10 under 35 USC § 102(b) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made over Stapleton in view of Heimbigner (as shown above).

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The Examiner can normally be reached on 8AM - 4PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business

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James F. Sugent
Patent Examiner, Art Unit 2116
April 29, 2007

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SUPERVISORY PATENT EXAMINER
4/30/07